

WHAT IS CLAIMED IS:

1 1. A method for transferring data in parallel from an external memory
2 device to an integrated circuit, the method comprising:
3 transferring a start read address from the integrated circuit to the external
4 memory device;
5 providing a clock signal generated by the integrated circuit to the external
6 memory device;
7 sequentially generating read addresses in response to the clock signal
8 beginning with the start read address using an address counter in the external memory device;
9 reading data stored in the external memory device at the read addresses; and
10 transferring the data in parallel from the external memory device to the
11 integrated circuit.

1 2. The method as defined in claim 1 further comprising:
2 resetting a read address to the start read address when an output enable signal
3 generated by the integrated circuit has a first voltage,
4 wherein the address counter increments the read address in response to the
5 clock signal when the output enable signal has a second voltage.

1 3. The method as defined in claim 1 wherein the external memory device
2 operates in sequential read mode when the clock signal toggles.

1 4. The method as defined in claim 1 wherein the external memory device
2 operates in sequential read mode when the integrated circuit sends a sequential read
3 command to the external memory device.

1 5. The method as defined in claim 1 wherein the integrated circuit is a
2 first programmable integrated circuit that is coupled in series with a plurality of cascaded
3 programmable integrated circuits, and data is transferred in parallel from the external
4 memory device to the cascaded programmable integrated circuits.

1 6. The method as defined in claim 5 wherein the first programmable
2 integrated circuit is a master device that controls the transfer of the data from the external
3 memory device to the cascaded programmable integrated circuits.

1 7. The method as defined in claim 1 wherein the integrated circuit is a
2 field programmable gate array and the data is configuration data.

1 8. The method as defined in claim 1 wherein the integrated circuit is a
2 programmable integrated circuit that is part of a digital system that includes a
3 microprocessor.

1 9. The method as defined in claim 1 wherein the data is transferred in
2 parallel from the external memory device to the integrated circuit along 8 parallel signal
3 lines.

1 10. The method as defined in claim 1 wherein the data is transferred in
2 parallel from the external memory device to the integrated circuit along 16 parallel signal
3 lines.

1 11. The method as defined in claim 1 wherein the external memory device
2 is a FLASH memory.

1 12. A system for transferring data to an integrated circuit, the system
2 comprising:
3 an integrated circuit that generates a start read address and a clock signal; and
4 an external memory device including an address counter that sequentially
5 generates read addresses beginning with the start read address in response to the clock signal,
6 that accesses data stored in a memory array at the read addresses, and that transfers the
7 accessed data along parallel signal lines to the integrated circuit.

1 13. The system according to claim 12 wherein the address counter resets a
2 read address to the start read address when an output enable signal generated by the
3 integrated circuit has a first voltage, and the address counter increments the read address in
4 response to the clock signal when the output enable signal has a second voltage.

1 14. The system according to claim 12 wherein the external memory device
2 operates in sequential read mode when the clock signal toggles.

1 15. The method as defined in claim 12 wherein the external memory
2 device operates in sequential read mode when the integrated circuit sends a sequential read
3 command to the external memory device.

1 16. The system according to claim 12 wherein the integrated circuit is a
2 first programmable integrated circuit that is coupled in series with a plurality cascaded
3 programmable integrated circuits, and data is transferred in parallel from the external
4 memory device to the cascaded programmable integrated circuits.

1 17. The system according to claim 16 wherein the first programmable
2 integrated circuit is a master device that controls the transfer of the data from the external
3 memory device to the cascaded programmable integrated circuits.

1 18. The system according to claim 12 wherein the integrated circuit is a
2 field programmable gate array and the data is configuration data.

1 19. The system according to claim 12 wherein the integrated circuit is a
2 programmable integrated circuit that is part of a digital system including a microprocessor.

1 20. The system according to claim 12 wherein the accessed data is
2 transferred in parallel from the external memory device to the integrated circuit along 8
3 parallel signal lines.

1 21. The system according to claim 12 wherein the accessed data is
2 transferred in parallel from the external memory device to the integrated circuit along 16
3 parallel signal lines.

1 22. The system according to claim 12 wherein the external memory device
2 is a FLASH memory.